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(54) **ACTIVE MATRIX ORGANIC LIGHT EMITTING DISPLAY (OLED) AND METHOD OF FABRICATION**

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(57) **ABSTRACT**

An organic light emitting display includes a substrate having a pixel driving circuit region and an opening region. A thin film transistor having source/drain electrodes is positioned on the pixel driving circuit region of the substrate. A passivation insulating layer is positioned on the source/drain electrodes to have a via hole for exposing one of the source/drain electrodes. A pixel electrode is positioned on a bottom surface of the via hole and in contact with the exposed source/drain electrode, and extends onto the passivation insulating layer. A first photosensitive organic insulating layer is positioned within the via hole in which the pixel electrode is formed to fill the via hole and to expose a portion of the pixel electrode around the via hole. An organic emission layer is positioned on the exposed pixel electrode.

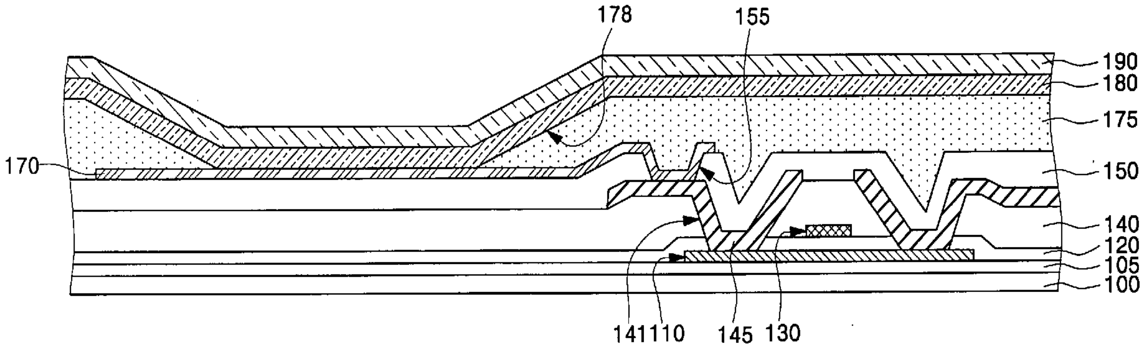


FIG. 1

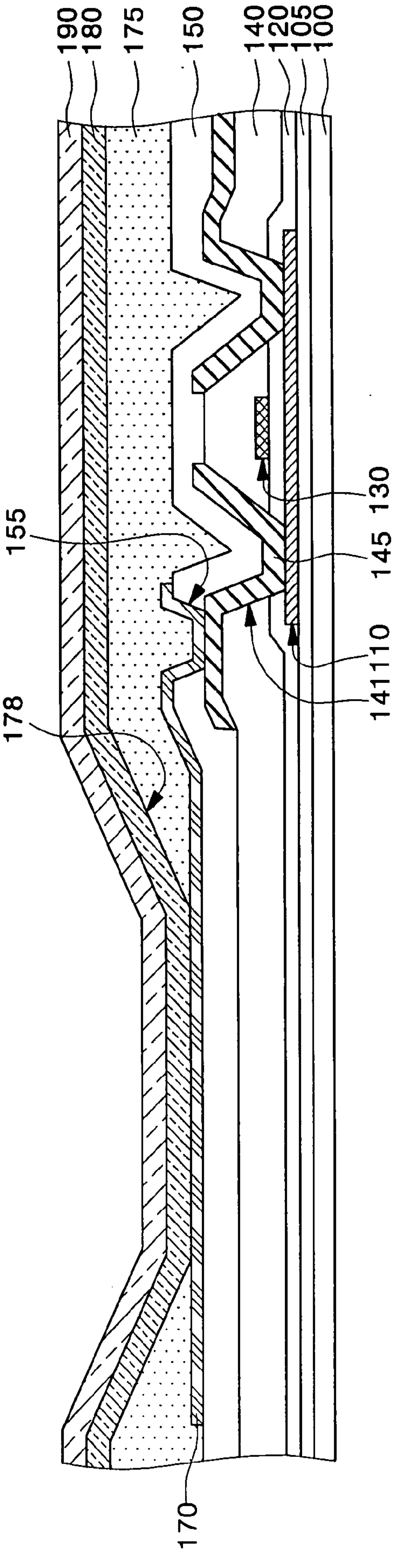


FIG. 2A

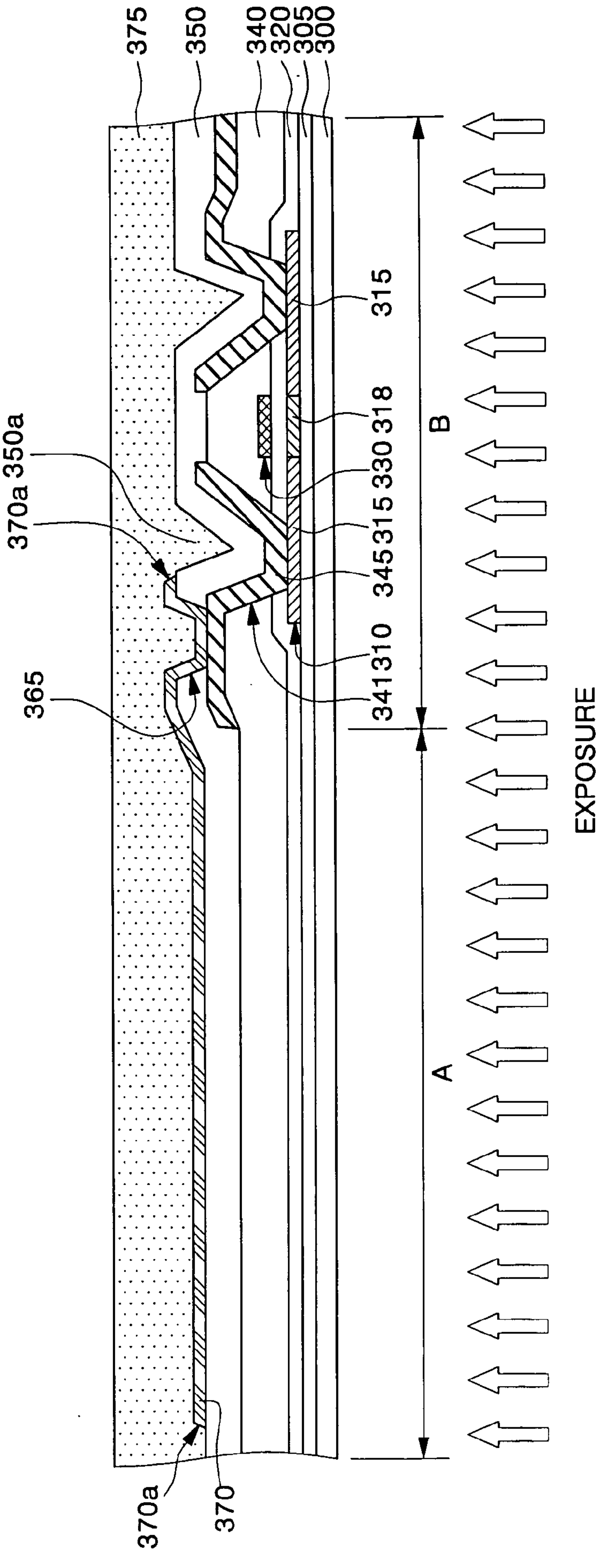

375
350
340
320
305
300
315
318
330
315
345
310
341
370a
350a
365
370a
370
B
A
EXPOSURE

FIG. 2B

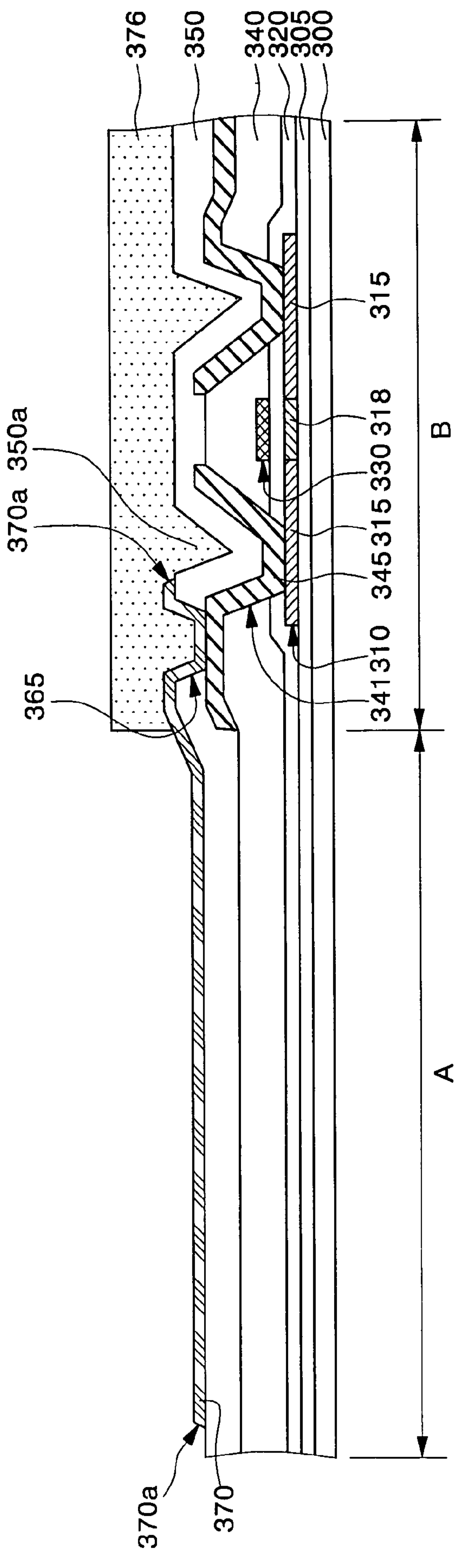
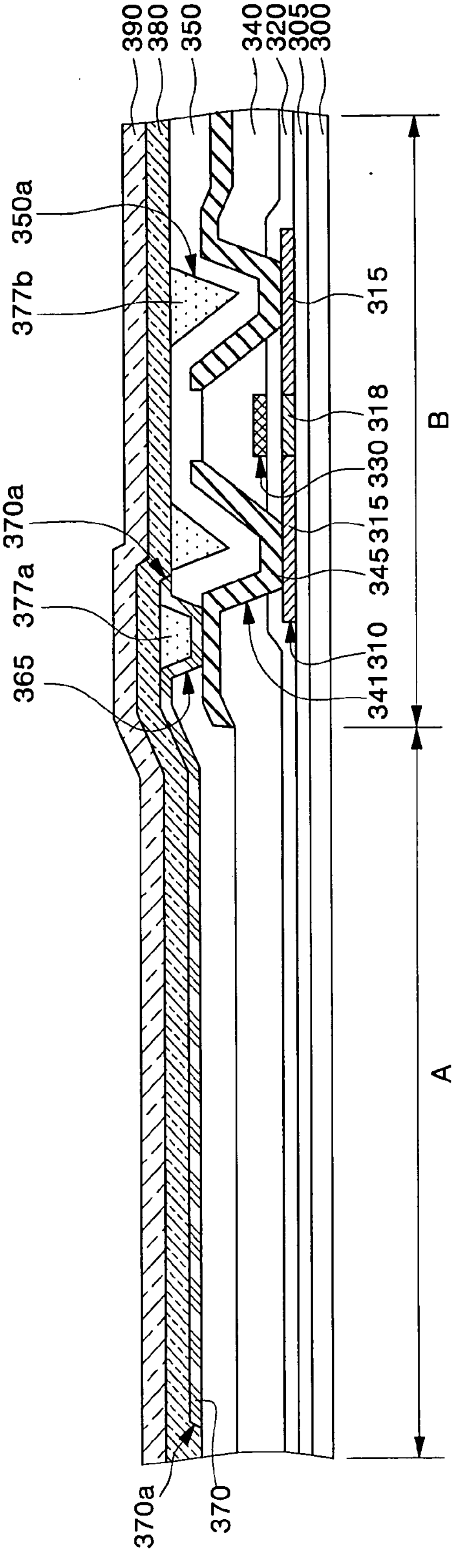

376
350
340
320
305
300
315
318
B
330
315
345
310
341
370a
350a
370a
365
A
370a
370

FIG. 2C


390
380
350
340
320
305
300
350a
377b
315
318
330
315
345
310
341
370a
377a
365
B
A
370a
370

ACTIVE MATRIX ORGANIC LIGHT EMITTING DISPLAY (OLED) AND METHOD OF FABRICATION

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. §119 from an application for ACTIVE MATRIX OLED AND METHOD FOR FABRICATING THE SAME earlier filed in the Korean Intellectual Property Office on Nov. 22, 2003 and there duly assigned Serial No. 2003-83391.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an Organic Light Emitting Display (OLED) and method of fabrication and, more particularly, to an Active Matrix OLED (AMOLED) and method of fabrication.

[0004] 2. Description of the Related Art

[0005] In general, an OLED is an emissive display in which a fluorescent organic compound is electrically excited to emit light therefrom. OLEDs can be classified into passive OLEDs and active OLEDs based on a driving scheme for driving N×M pixels arranged in a matrix form. The AMOLED has a lower power consumption than the passive matrix OLED so that it is advantageously suitable for implementing a large display area thereof and has high resolution.

[0006] An AMOLED includes a buffer layer formed on an insulating substrate. An active layer, a gate insulating layer, a gate electrode, an interlayer, and source/drain electrodes are formed on the buffer layer of the insulating layer using typical methods. The source/drain electrodes are in contact with the active layer through a contact hole formed within the interlayer. The active layer, the gate insulating layer, the gate electrode, and the source/drain electrode form a thin film transistor. A passivation layer is formed over the entire surface of the substrate including the thin film transistor, and a via hole for exposing one of the source/drain electrodes is formed within the passivation layer. The passivation layer is an inorganic layer and has bad planarization properties so that it has a groove resulted from patterns below the passivation layer, especially due to topology of the contact hole.

[0007] A pixel electrode is then formed to be in contact with the source/drain electrode exposed within the via hole. Since the pixel electrode is formed along the bottom and side walls of the via hole, it is bent within the via hole. A pixel defining layer is then formed to cover the bent pixel electrode within the via hole such that the pixel defining layer has an opening for exposing the pixel electrode at a position spaced apart from the via hole. Then, an organic emission layer is formed on the pixel electrode exposed within the opening, and an opposite electrode is formed on the organic emission layer. The pixel electrode, the organic emission layer, and the opposite electrode form an organic light emitting diode, which is connected to the thin film transistor through the via hole so that it is driven by the thin film transistor.

[0008] In the method of fabricating the OLED, the pixel defining layer acts to protect the organic emission layer from being positioned on the bent pixel electrode within the via hole, so that deterioration due to the bent organic emission layer can be prevented. In addition, the topology due to patterns below the passivation layer, especially the topology due to the contact hole can be relaxed to prevent the organic emission layer from being bent or broken above the contact hole.

[0009] The pixel defining layer is generally formed of a photosensitive organic insulating layer having good planarization properties, and the photosensitive organic insulating layer contains a sensitizer. When the organic light emitting display is driven, the sensitizer can take a form of outgas to cause the deterioration of the organic emission layer in contact with the pixel defining layer.

SUMMARY OF THE INVENTION

[0010] The present invention provides an organic light emitting display and method of fabrication, which can minimize the deterioration of an organic emission layer due to outgas emitted from a photosensitive layer and at the same time can also prevent the deterioration due to bending of the organic emission layer.

[0011] In accordance with one aspect of the present invention, a display is provided comprising: a substrate including a pixel driving circuit region and an opening region; a thin film transistor positioned on the pixel driving circuit region and having source/drain electrodes; an insulating layer positioned on the source/drain electrodes and having a via hole adapted to expose one of the source/drain electrodes; a pixel electrode contacting the exposed source/drain electrode in the via hole and extending onto the insulating layer; a first photosensitive layer pattern positioned within the via hole in which the pixel electrode is arranged and adapted to expose a portion of the pixel electrode adjacent to the via hole; and an organic emission layer positioned on the exposed pixel electrode.

[0012] The first photosensitive layer pattern preferably comprises one of an acrylic-based polymer and an imide-based polymer.

[0013] The insulating layer preferably comprises an inorganic layer.

[0014] The inorganic layer preferably comprises a silicon nitride layer.

[0015] The first photosensitive layer pattern preferably exposes the portion of the pixel electrode around the via hole.

[0016] The insulating layer preferably comprises a groove, and wherein the display preferably further comprises a second photosensitive layer pattern adapted to fill the groove of the insulating layer.

[0017] The second photosensitive layer pattern preferably comprises one of an acrylic-based polymer and an imide-based polymer.

[0018] The pixel electrode preferably comprises one of Indium Tin Oxide (ITO) and Indium Zinc Oxide (IZO).

[0019] The pixel electrode preferably includes a tapered edge.

[0020] The tapered edge of the pixel electrode preferably includes a taper angle less than or equal to 20 degrees.

[0021] In accordance with another aspect of the present invention, a method of fabricating a display is provided, the method comprising: preparing a substrate to include a pixel driving circuit region and an opening region, the substrate having an upper surface and a lower surface; forming a thin film transistor having source/drain electrodes on the upper surface of the substrate of the pixel driving circuit region; forming an insulating layer on the source/drain electrodes; forming a via hole to expose one of the source/drain electrodes under the insulating layer; forming a pixel electrode contacting the exposed source/drain electrode within the via hole and extending onto the insulating layer; forming an photosensitive layer on the substrate including the pixel electrode; irradiating light onto the lower surface of the substrate to expose the photosensitive layer; developing the exposed photosensitive layer to expose the pixel electrode of the opening region; etching back the developed photosensitive layer to form a first photosensitive layer pattern within the via hole and to expose a portion of the pixel electrode adjacent to the via hole; and forming an organic emission layer on the exposed pixel electrode.

[0022] Forming the insulating layer preferably comprises forming an inorganic layer.

[0023] Forming the inorganic layer preferably comprises forming a silicon nitride layer.

[0024] Forming the insulating layer preferably includes forming a groove therein, and the method preferably further comprises forming a second photosensitive layer pattern to fill the groove when the developed photosensitive layer is etched back.

[0025] The pixel electrode is preferably formed of one of Indium Tin Oxide (ITO) and Indium Zinc Oxide (IZO).

[0026] The pixel electrode is preferably formed to have a tapered edge.

[0027] The tapered edge of the pixel electrode preferably has a taper angle less than or equal to 20 degrees.

[0028] The photosensitive layer is preferably formed of one of an acrylic-based polymer and an imide-based polymer.

[0029] The photosensitive layer is preferably formed by a spin coating method.

[0030] The photosensitive layer is preferably etched back by ashing.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

[0032] **FIG. 1** is a cross-sectional view of an AMOLED and method of fabrication; and

[0033] **FIG. 2A** to **FIG. 2C** are cross-sectional views of an AMOLED and method of fabrication in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0034] **FIG. 1** is a cross-sectional view of an AMOLED and method of fabrication.

[0035] Referring to **FIG. 1**, a buffer layer **105** is formed on an insulating substrate **100**. An active layer **110**, a gate insulating layer **120**, a gate electrode **130**, an interlayer **140**, and source/drain electrodes **145** are formed on the buffer layer **105** of the insulating layer **100**. The source/drain electrodes **145** are in contact with the active layer **110** through a contact hole **141** formed within the interlayer **140**. The active layer **110**, the gate insulating layer **120**, the gate electrode **130**, and the source/drain electrode **145** form a thin film transistor. A passivation layer **150** is formed over the entire surface of the substrate **100** including the thin film transistor, and a via hole **155** for exposing one of the source/drain electrodes **145** is formed within the passivation layer **150**. The passivation layer **150** is an inorganic layer and has bad planarization properties so that it has a groove resulting from patterns below the passivation layer **150**, especially due to the topology of the contact hole **141**.

[0036] A pixel electrode **170** is then formed to contact the source/drain electrode **145** exposed within the via hole **155**. Since the pixel electrode **170** is formed along the bottom and side walls of the via hole **155**, it is bent within the via hole **155**. A pixel defining layer **175** is then formed to cover the bent pixel electrode **170** within the via hole **155** such that the pixel defining layer **175** has an opening **178** for exposing the pixel electrode **170** at a position spaced apart from the via hole **155**. Then, an organic emission layer **180** is formed on the pixel electrode **170** exposed within the opening **178**, and an opposite electrode **190** is formed on the organic emission layer **180**. The pixel electrode **170**, the organic emission layer **180**, and the opposite electrode **190** form an organic light emitting diode, which is connected to the thin film transistor through the via hole **155** so that it is driven by the thin film transistor.

[0037] In the method of fabricating the OLED, the pixel defining layer **175** acts to protect the organic emission layer **180** from being positioned on the bent pixel electrode **170** within the via hole **150**, so that deterioration due to the bent organic emission layer **180** can be prevented. In addition, the topology due to patterns below the passivation layer **150**, especially the topology due to the contact hole **141** can be relaxed to prevent the organic emission layer **180** from being bent or broken above the contact hole **141**.

[0038] The pixel defining layer **175** is generally formed of a photosensitive organic insulating layer having good planarization properties, and the photosensitive organic insulating layer contains a sensitizer. When the OLED is driven, the sensitizer can take a form of an outgas to cause the deterioration of the organic emission layer **180** in contact with the pixel defining layer.

[0039] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which an exemplary embodiment of the present invention is shown. The present invention, however, can be embodied in different forms and should not be construed as being limited to the embodiment set forth herein. Rather, the exemplary embodiment is provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present invention to those skilled in the art.

[**0040**] In the following discussion, a layer described as being formed on another layer or on a substrate is to be interpreted as meaning that the layer can be formed directly on another layer or on the substrate or that a third layer can be interposed between the layer and another layer or the substrate. Like numbers refer to like elements throughout the specification and drawings.

[**0041**] **FIG. 2A** to **FIG. 2C** are cross-sectional views of an AMOLED and method of fabrication in accordance with an embodiment of the present invention. The OLED has at least one unit pixel, and these figures are limited to show the unit pixel of the OLED.

[**0042**] Referring to **FIG. 2A**, a substrate **300** having an opening region A and a pixel driving circuit region B is prepared. The substrate **300** has an upper surface and a lower surface. The substrate **300** can be an insulating substrate. The substrate **300** is preferably a transparent substrate formed of glass or plastic. A buffer layer **305** is then formed on the upper surface of the substrate **300**. The buffer layer **305** acts to protect a thin film transistor to be formed in a subsequent process from impurities emitted by the substrate **300**, and can be formed of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer or a stacked layer thereof.

[**0043**] Subsequently, an active layer **310** is formed on the pixel driving circuit region B of the substrate **300** where the buffer layer **305** has already been formed. The active layer **310** can be formed of amorphous silicon or polycrystalline silicon, and is preferably formed of polycrystalline silicon. A gate insulating layer **320** is formed over the upper surface of the substrate including the active layer **310**, and a gate electrode **330** is formed on the gate insulating layer **320** at a position corresponding to a predetermined region of the active layer **310**. Impurities are doped into the active layer **310** using the gate electrode **330** as a mask to form source/drain regions **315** in the active layer while a channel region **318** is defined to be interposed between the source/drain regions **315**. An interlayer **340** is formed over the upper surface of the substrate including the gate electrode **330**. The interlayer **340** can be formed of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer or a stacked layer thereof. Contact holes **341** for exposing respective source/drain regions **315** are then formed within the interlayer **340**. A conductive layer is deposited on the interlayer **340** and the source/drain regions **315** exposed within the contact holes **341**. The deposited conductive layer is patterned, thereby forming source/drain electrodes **345**. The source/drain electrodes **345** are respectively in contact with the source/drain regions **315** exposed within the contact holes **341**. The active layer **310**, the gate electrode **330**, and the source/drain electrodes **345** form the thin film transistor.

[**0044**] Then, an insulating layer **350** is formed on the source/drain electrodes **345**. The insulating layer **350** can be a passivation layer **350**. The passivation layer **350** can be an inorganic layer. The passivation layer **350** is preferably a silicon nitride layer. The passivation layer **350** not only protects the thin film transistor below the passivation layer **350** but also passivates a dangling bond present in a crystal grain boundary of the active layer **310** when the active layer **310** is formed of a polycrystalline silicon. Such a passivation layer **350** has bad planarization properties, so that it has a groove **350***a* resulting from a topology due to patterns below the passivation layer **350**, especially due to the contact hole **341**.

[**0045**] A via hole **365** is then formed within the passivation layer **350** to expose one of the source/drain electrodes **345**. A transparent conductive layer is deposited on the passivation layer **350**, and is patterned to form a pixel electrode **370**. The pixel electrode **370** is in contact with the exposed source/drain electrode **345** in the via hole **365**, specifically at the bottom of the via hole **365**. The pixel electrode **370** extended onto the passivation layer **350**. The pixel electrode **370** is preferably formed to have a tapered edge **370***a* when the deposited transparent conductive layer is patterned. More preferably, the taper angle is 20° or less. The transparent conductive layer, namely, the pixel electrode **370** is preferably formed of Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO).

[**0046**] A photosensitive layer **375** is then formed on the substrate including the pixel electrode **370** such that the photosensitive layer **375** fills the via hole **365** where the pixel electrode **370** is formed and the groove **350***a*. It is preferable for the photosensitive layer **370** to have superior planarization properties. The photosensitive layer **370** having superior planarization properties can relax the topology of the passivation layer **350** to have a planarized surface. For this reason, the photosensitive layer **375** is preferably an organic layer. The photosensitive layer **375** is a positive type so that it has a property that it is changed into a material to be dissolved in a developing solution when exposed to light. The photosensitive layer **375** is preferably formed of an acrylic-based polymer or an imide-based polymer (polyimide). Furthermore, the photosensitive layer **375** can be formed on the substrate using a spin-coating method.

[**0047**] Then, light is irradiated onto the lower surface of the substrate **300** where the photosensitive layer **375** has already been formed to perform back exposure to the photosensitive layer **375**. On the opening region A of the substrate **300**, the buffer layer **305**, the gate insulating layer **320**, the interlayer **340**, and the passivation layer **350** are sequentially deposited, so that the light incident from the lower surface of the substrate **300** can be transmitted. Thus, the photosensitive layer **375** formed on the passivation layer **350** of the opening region A is exposed to the light. On the pixel driving circuit region B of the substrate, the active layer **310**, the gate electrode **330**, gate wiring (not shown), the source/drain electrodes **345**, data wiring (not shown), and power supply wiring (not shown) are disposed, wherein the active layer **310** is formed of silicon, and the gate electrode **330**, the source/drain electrodes **345**, and the data wiring and power supply wiring are formed of metal so that the light can not be transmitted therethrough. Thus, the photosensitive layer **375** formed on the passivation layer **350** of the pixel driving circuit region B, is not exposed to the light incident from the lower surface of the substrate **300**. As a result, a portion of the photosensitive layer **375** exposed to the light, namely, a portion on the opening region A is changed into a material that can be dissolved in a developing solution whereas the photosensitive layer **375** on the pixel driving circuit region B is not changed.

[**0048**] Referring to **FIG. 2B**, the photosensitive layer **375** is developed using the developing solution. In this case, the photosensitive layer **375** on the opening region A is dissolved by the developing solution and removed, so that the pixel electrode **370** on the opening region A is exposed. A developed photosensitive layer **376** is disposed on the pixel driving circuit region B including the upper portion of the via hole **365**.

[0049] Referring to **FIG. 2C**, the developed photosensitive layer **376** is etched back until the passivation layer **350** is exposed. The developed photosensitive layer **376** is anisotropically etched from its upper portion by the etch back, thereby forming a first photosensitive layer pattern **377***a* and a second photosensitive layer pattern **377***b*.

[0050] The first photosensitive layer pattern **377***a* is positioned within the via hole **365**, specifically, to fill the via hole **365** where the pixel electrode **370** is formed, and to expose a portion of the pixel electrode adjacent the via hole **365**. The first photosensitive layer pattern **377***a* expose the pixel electrode **370** around the via hole. The second photosensitive layer pattern **377***b* fills the groove **350***a* of the passivation layer **350** to expose the passivation layer **350** of the pixel driving circuit region B. As a result, both the upper portion of the via hole **365** and the upper portion of the groove **350***a* can be planarized.

[0051] The etchback can be performed by ashing. Gases used for the ashing can include O2, Ar, CF4, and SF6. When the ashing is performed, upper portions of the first and second photosensitive layer patterns **377***a* and **377***b* exposed to the ashing gas can be cured to reduce outgassing.

[0052] Then, an organic emission layer **380** is formed over the upper surface of the substrate including the first and second photosensitive layer patterns **377***a* and **377***b*. As a result, the organic emission layer **380** is formed not only on the exposed pixel electrode **370** but also on an edge **370***a* of the pixel electrode **370**. As mentioned above, the pixel electrode **370** is formed to have the tapered edge **370***a*, so that deterioration of the organic emission layer **380** due to bias focused on the edge **370***a* of the pixel electrode **370** can be suppressed. The organic emission layer **380** can be patterned per unit pixel so as to implement a full color OLED. The organic emission layer **380** can be patterned by a laser induced thermal imaging method, a vacuum deposition method using a shadow mask, or the like. An opposite electrode **390** is then formed on the organic emission layer **380**. The opposite electrode **390** can be formed over the entire surface of the substrate. The pixel electrode **370**, the organic emission layer **380**, and the opposite electrode **390** form an organic light emitting diode, which is connected to the thin film transistor through the via hole **365** to be driven by the thin film transistor.

[0053] As mentioned above, areas occupied by the photosensitive layer patterns **377***a* and **377***b* can be minimized, and at the same time the upper portion of the via hole **365** as well as the groove **377***b* can also be planarized by the photosensitive layer patterns **377***a* and **377***b*. Such a configuration can not only suppress the deterioration of the organic emission layer **380** due to the outgas emitted from the photosensitive layer but can also suppress the deterioration due to the bending of the opposite electrode **390** and the organic emission layer **380**. In addition, the photosensitive layer **377** is exposed to light incident from the lower surface of the substrate, wherein such exposure on the photosensitive layer. **377** is performed using the metal wiring and the active layer **310** on the pixel driving circuit region B as a mask, so that the number of masks can be reduced as compared to performing an exposure on the upper surface of the substrate using another photomask.

[0054] In accordance with the present invention as mentioned above, deterioration of the organic emission layer due to outgas emitted from a photosensitive layer can be minimized, and at the same time the deterioration due to bending of the opposite electrode and the organic emission layer can also be prevented.

[0055] While the present invention has been described with reference to a particular embodiment, it is understood that the disclosure has been made for purpose of illustrating the invention by way of example and is not to be construed as limiting the scope of the present invention. One skilled in the art can modify the present invention without departing from the scope and spirit of the present invention.

What is claimed is:

1. A display, comprising:

a substrate including a pixel driving circuit region and an opening region;

a thin film transistor positioned on the pixel driving circuit region and having source/drain electrodes;

an insulating layer positioned on the source/drain electrodes and having a via hole adapted to expose one of the source/drain electrodes;

a pixel electrode contacting the exposed source/drain electrode in the via hole and extending onto the insulating layer;

a first photosensitive layer pattern positioned within the via hole in which the pixel electrode is arranged and adapted to expose a portion of the pixel electrode adjacent to the via hole; and

an organic emission layer positioned on the exposed pixel electrode.

2. The display as claimed in claim 1, wherein the first photosensitive layer pattern comprises one of an acrylic-based polymer and an imide-based polymer.

3. The display as claimed in claim 1, wherein the insulating layer comprises an inorganic layer.

4. The display as claimed in claim 3, wherein the inorganic layer comprises a silicon nitride layer.

5. The display as claimed in claim 1, wherein the first photosensitive layer pattern exposes the portion of the pixel electrode around the via hole.

6. The display as claimed in claim 1, wherein the insulating layer comprises a groove, and wherein the display further comprises a second photosensitive layer pattern adapted to fill the groove of the insulating layer.

7. The display as claimed in claim 6, wherein the second photosensitive layer pattern comprises one of an acrylic-based polymer and an imide-based polymer.

8. The display as claimed in claim 1, wherein the pixel electrode comprises one of Indium Tin Oxide (ITO) and Indium Zinc Oxide (IZO).

9. The display as claimed in claim 1, wherein the pixel electrode includes a tapered edge.

10. The display as claimed in claim 9, wherein the tapered edge of the pixel electrode includes a taper angle less than or equal to 20 degrees.

11. A method of fabricating a display, the method comprising:

preparing a substrate to include a pixel driving circuit region and an opening region, the substrate having an upper surface and a lower surface;

forming a thin film transistor having source/drain electrodes on the upper surface of the substrate of the pixel driving circuit region;

forming an insulating layer on the source/drain electrodes;

forming a via hole to expose one of the source/drain electrodes under the insulating layer;

forming a pixel electrode contacting the exposed source/drain electrode within the via hole and extending onto the insulating layer;

forming an photosensitive layer on the substrate including the pixel electrode;

irradiating light onto the lower surface of the substrate to expose the photosensitive layer;

developing the exposed photosensitive layer to expose the pixel electrode of the opening region;

etching back the developed photosensitive layer to form a first photosensitive layer pattern within the via hole and to expose a portion of the pixel electrode adjacent to the via hole; and

forming an organic emission layer on the exposed pixel electrode.

12. The method as claimed in claim 11, wherein forming the insulating layer comprises forming an inorganic layer.

13. The method as claimed in claim 12, wherein forming the inorganic layer comprises forming a silicon nitride layer.

14. The method as claimed in claim 11, wherein forming the insulating layer includes forming a groove therein, and wherein the method further comprises forming a second photosensitive layer pattern to fill the groove when the developed photosensitive layer is etched back.

15. The method as claimed in claim 11, wherein the pixel electrode is formed of one of Indium Tin Oxide (ITO) and Indium Zinc Oxide (IZO).

16. The method as claimed in claim 11, wherein the pixel electrode is formed to have a tapered edge.

17. The method as claimed in claim 16, wherein the tapered edge of the pixel electrode has a taper angle less than or equal to 20 degrees.

18. The method as claimed in claim 11, wherein the photosensitive layer is formed of one of an acrylic-based polymer and an imide-based polymer.

19. The method as claimed in claim 11, wherein the photosensitive layer is formed by a spin coating method.

20. The method as claimed in claim **11**, wherein the photosensitive layer is etched back by ashing.

* * * * *

专利名称(译)	有源矩阵有机发光显示器（OLED）和制造方法		
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[标]申请(专利权)人(译)	朴相IL KIM IEE GON		
申请(专利权)人(译)	朴相IL KIM IEE-GON		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	PARK SANG IL KIM IEE GON		
发明人	PARK, SANG-IL KIM, IEE-GON		
IPC分类号	H05B33/10 G09F9/30 H01L27/32 H01L29/04 H01L51/50 H01L51/52 H05B33/00 H05B33/08 H05B33/12 H05B33/14 H05B33/22 H05B33/26 H05B33/28		
CPC分类号	H01L27/3246 H01L51/5206 H01L27/3258 H01L27/3248 H01L51/5209		
优先权	1020030083391 2003-11-22 KR		
其他公开文献	US7692197		
外部链接	Espacenet USPTO		

摘要(译)

有机发光显示器包括具有像素驱动电路区域和开口区域的基板。具有源/漏电极的薄膜晶体管位于基板的像素驱动电路区域上。钝化绝缘层位于源/漏电极上以具有用于暴露源/漏电极之一的通孔。像素电极位于通孔的底表面上并与暴露的源/漏电极接触，并延伸到钝化绝缘层上。第一光敏有机绝缘层位于通孔内，其中形成像素电极以填充通孔并使像素电极的一部分暴露在通孔周围。有机发光层位于暴露的像素电极上。